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QCA Binary Adder Implementation on FPGA

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Abstract*:The area and complexity are the major issues in circuit design. Here, adder design is proposed based on Quantum dot Cellular Automata (QCA) that reduces number of QCA cells and area compare to previous designs. The quantum dot cellular automata can implement digital circuits with faster speed, smaller size and low power consumption. The QCA cell is a basic building block of nanotechnology that can be used to make gates, wires and memories. The basic logic circuits used in this technology are the inverter and the Majority Gate (MG), using this other logical circuits can be designed. In this project, stop Watch timer is designed and analyzed based upon adder and is implemented on FPGA. The proposed method can be used to minimize area and complexity. These circuits were designed by majority gate and implemented by QCA cells.*

Keywords:*quantum dot cellular automata,Carry Look Ahead Adder,one-bit QCA adder*

I. Introduction

1 general

In electronics, an adder or summer is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit(s), but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Although adders can be constructed for many numerical representations, such as binary-coded decimal or excess-3, the most common adders operate on binary numbers. In cases where two's complement or ones' complement is being used to represent negative numbers, it is trivial to modify an adder into an adder–subtractor. Other signed number representations require a more complex adder.

1.1half adder

The **half adder** adds two single binary digits A and B. It has two outputs, sum (S) and carry (C). The carry signal represents an overflow into the next digit of a multi-digit addition. The value of the sum is 2C + S. The simplest half-adder design, pictured on the right, incorporates an XOR gate for S and an AND gate for C. With the addition of an OR gate to combine their carry outputs, two half adders can be combined to make a full adder. The half-adder adds two inputs bits and generate carry and sum which are the two outputs of half-adder.

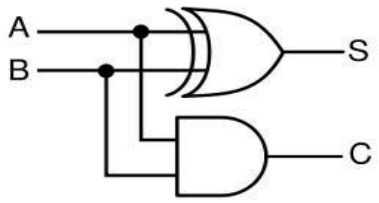

Fig 1 half adder circuit

1.2Full adder

A **full adder** adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as A, B, and Cin; A andB are the operands, and Cin is a bit carried in from the next less significant stage. The full-adder is usually a component in a cascade of adders, which add 8, 16, 32, etc.

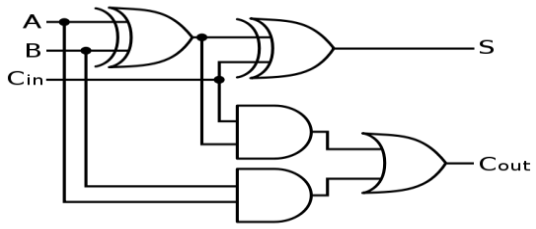

Fig 2 Full adder circuit

1.3Ripple-carry adder

It is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a Cin, which is the Coutof the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder. The **ripple carry adder (RCA)** provides a slow and efficient method for adding two binary numbers. The comparative study of these adders gives better scope thus by cascading n-full adder we get n-bit RCA .For high speed operation two types of full adders are used .The carryout of Jth full adder is used as the carry in the (J+1)th full adder as shown. The carry propagation delay for each full adder is the times from the application of the input carry until the output carry is valid.

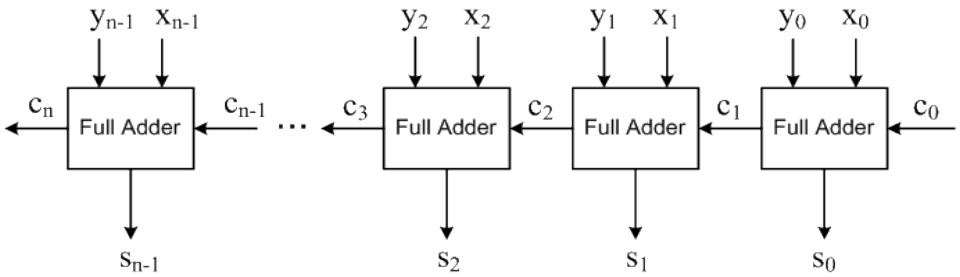

Fig.3n bit ripple carry adder

1.4Carry-look ahead adders

To reduce the computation time, engineers devised faster ways to add two binary numbers by using carry-look ahead adders. They work by creating two signals (P and G) for each bit position, based on whether a carry is propagated through from a less significant bit position (at least one input is a '1'), generated in that bit position (both inputs are '1'), or killed in that bit position (both inputs are '0'). In most cases, P is simply the sum output of a half-adder and G is the carry output of the same adder. After P and G are generated the carries for every bit position are created. Some advanced carry-look ahead architectures are the Manchester carry chain, Brent–Kung adder, and the Kogge–Stone adder.

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Some other multi-bit adder architectures break the adder into blocks. It is possible to vary the length of these blocks based on the propagation delay of the circuits to optimize computation time. These block based adders include the carry-skip (or carry-bypass) adder which will determine P and G values for each block rather than each

bit, and the carry select adder which pre-generates the sum and carry values for either possible carry input (0 or 1) to the block, using multiplexers to select the appropriate result when the carry bit is known.

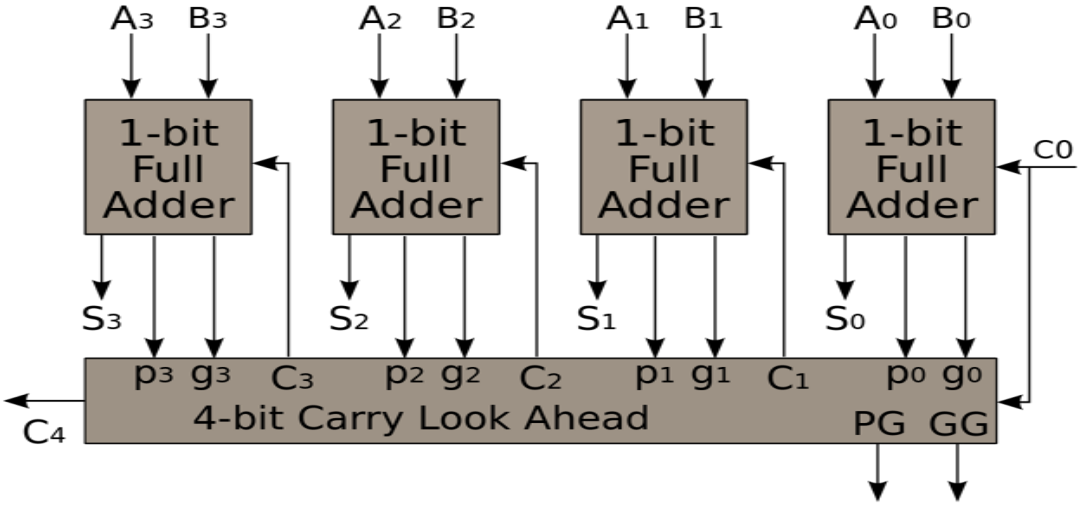

Fig 4carry look ahead adder

II. Existing Method

In Existing system one-bit QCA adder structure is based on a new algorithm that requires only three majority gates and two inverters for the QCA addition. By connecting n one-bit QCA adders, we can obtain an

n-bit carry look-ahead adder with the reduced hardware while retaining the simple clocking scheme and parallel structure of the original carry look-ahead approach.

The Existing adder design follows that of a conventional ripple carry adder, but with a new layout optimized to QCA technology. The proposed adder design shows that a very high delay can be obtained with an optimized layout. This is in contrast to the conventional ripple carry adder. To avoid confusion, the new layout is referred to as the Carry Flow Adder (CFA) here. In this Carry Flow Adder occupy more Number of gate Counts and More Delay.

In this paper, a novel QCA adder design has been presented that reduces the number of QCA cells in comparison to previously reported designs. The proposed one-bit QCA adder structure is based on a new algorithm that requires only three majority gates and two inverters for QCA addition. By connecting n proposed one-bit QCA adders, we can obtain an n-bit carry look ahead adder with the reduced hardware while retaining the simpler clocking scheme and parallel structure of the original approach.

III. Proposed Method

To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two n-bit addends $A = a_{n-1}, \ldots, a_0$ and $B = b_{n-1}, \ldots, b_0$ and suppose that for the i^{th} bit position (with $i = n - 1, \ldots, 0$) the auxiliary propagate and generate signals, namely $p_i = a_i + b_i$ and $g_i = a_i \cdot b_i$, are computed. cibeing the carry produced at the generic (i−1) th bit position, the carry signal c_i+2, furnished at the (i+1)th bit position, can be computed using the conventional CLA logic reported

$$C_{i+2} = g_{i+1} + p_{i+1} \cdot g_i + p_{i+1} \cdot p_i \cdot c_i$$

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The latter can be rewritten as given in $c_{i+2} = M(M(a_{i+1}, b_{i+1}, g_i)\ M(a_{i+1}, b_{i+1}, p_i)\ c_i)$. In this way, the RCA action, needed to propagate the carry $c_i$through the two subsequent bit positions, requires only one MG. Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation. In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA.

The proposed n-bit adder is then implemented by cascading n/2 2-bit modules as shown in Sum Chain. Having assumed that the carry-in of the adder is $c_{in} = 0$, the signal p_0 is not required and the 2-bit module used at the least significant bit position is simplified. The sum bits are finally computed as shown in Carry Chain.

3.1 module's

Majority QCA

Sum chain

Carry chain

3.2 module description

3.2.1Majority qca

The fundamental logic gates inherently available within the QCA technology are the inverter and the MG. Given three inputs a, b, and c, the MG performs the logic function reported in equation provided that all input cells are associated to the same clock signal clkx (with x ranging from 0 to 3), whereas the remaining cells of the MG are associated to

$$M(abc) = a \cdot b + a \cdot c + b \cdot c.$$

The latter can be rewritten as given in c i+2 = M (M (ai+1, bi+1, gi) M (ai+1, bi+1, pi) ci). In this way, the RCA action, needed to propagate the carry ci through the two subsequent bit positions, requires only one MG. Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation. In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA. The proposed n-bit adder is then implemented by cascading n/2

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3.2.2Sum chain

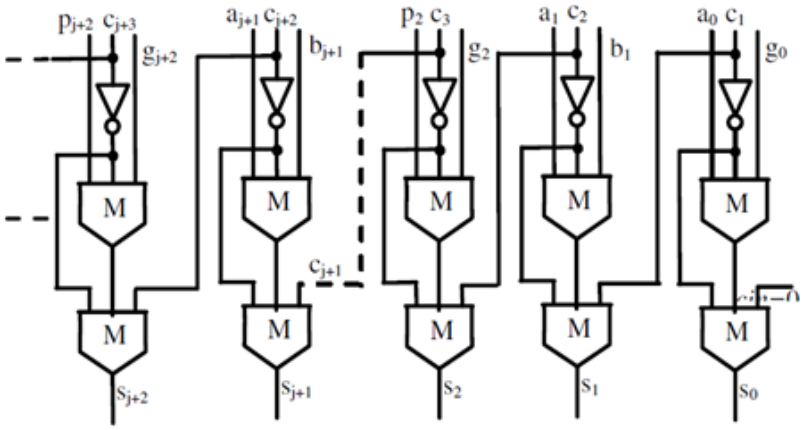

Fig 5sum chain

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3.2.3Carry chain

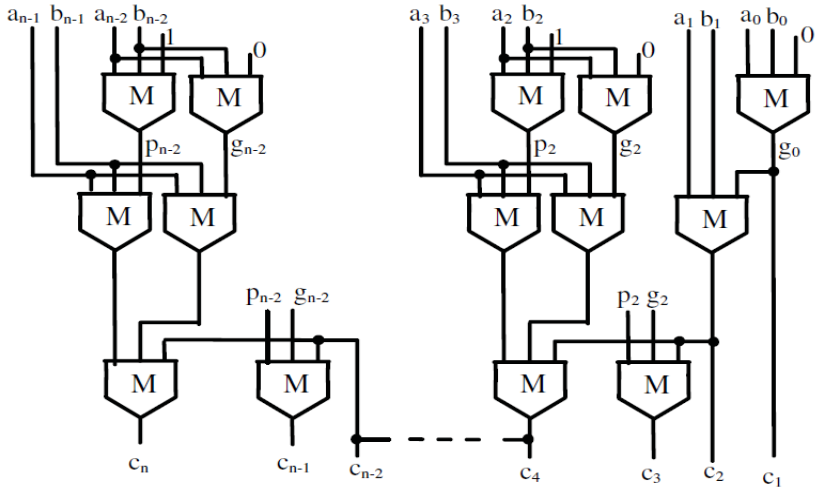

Fig 6 Carry Chain

IV. Qcaimplementation

There have been several proposals for physically implementing QCA. Micro-sized QCA devices have been fabricated with metal which operate at 50 mK and an extensive literature has been reported on developing molecular implementations of QCA. Magnetic QCA (MQCA) has been investigated and fabricated for room temperature operation. In this section, a brief background on Metal, Molecular, and Magnetic QCA is provided.

4.1metal qca

In, an experimental demonstration of a basic QCA cell it has been proposed that this device is composed of four aluminum islands (as dots) connected with aluminum-oxide tunnel junctions and capacitors. The area of the tunnel junctions determines the island capacitance (the charging energy of the dots) and hence, the operating temperature of the device. The device has an area of approximately 60 ×60nm^2 and is mounted on a surface at 10mK temperature. The device has been fabricated using Electron Beam Lithography (EBL) and dual shadow evaporation on an oxidized silicon wafer. The simplified schematic diagram of this cell is shown in Figure 3.7. The aluminum dots are located at D1 through D4, coupled by tunnel junctions. The two dots (E1 and E2) are SET electrometers for sensing the output. Figure 3.8 shows the scanning electron micrograph of this QCA cell.

Experiments have confirmed that switching of electrons in a c ell can control the position of electrons in another cell. In basic logic circuits made of these cells have been demonstrated. Sequential circuits have also

been fabricated using metal tunnel junction technology; the operation of a QCA latch and a two-bit shift register have been demonstrated in and implemented in. Figure 3.9 illustrates the schematic and electrical diagrams of a QCA latch. This device consists of three floating micron-size metal dots (D1-D_3), connected in series by multiple tunnel junctions (MTJ) and controlled by capacitively coupled gates. The electrometer (E_1), the signals ($-V_{IN}$, $+V_{IN}$), and the clock (V_C) are coupled to the dots. The operating temperature of these devices is 70mK. It is predicted that molecular scale (~ 2nm) will yield room temperature for QCA.

A semiconductor implementation of QCA is advantageous due to well under-stood behavior of existing semiconductors for which several tools and techniques have been already developed. However, fabrication processes

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Are not suitable to mass produce QCA cells of sufficiently small dimensions (few nanometers) for operating at room temperature

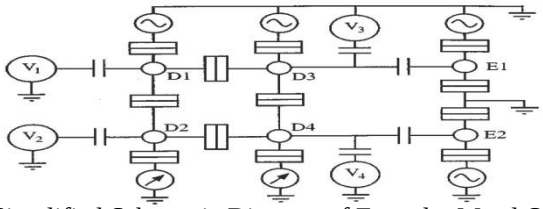

Fig 7 Simplified Schematic Diagram of Four-dot Metal QCA Cell

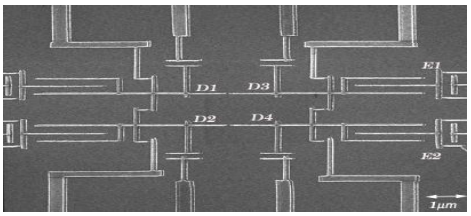

Fig 8 Scanning Electron Micrograph of the QCA Device

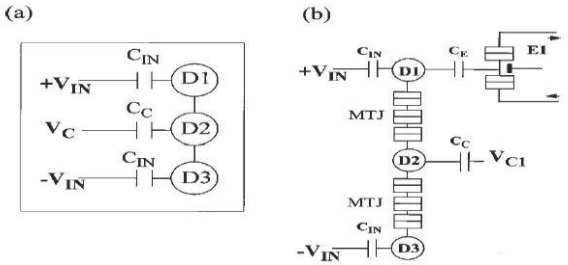

Fig 9a) Schematic and b) Electrical Diagrams of Half Cell QCA Latch

4.2power gain and dissipation

Energy dissipation causes a signal to degrade from stage to stage through its propagation path and eventually, this may result in a signal loss in the thermal background. A power supply and transistors are utilized in conventional CMOS circuits to restore the energy lost to dissipative processes. In QCA circuits, energy is restored by the clocking process and related electric field; when the signal strength in a QCA cell is reduced, the electric field provides additional energy to deliver copies of the cell's signal to the neighboring cells, while clocking takes place.Recently QCA has been advocated as a technology for reversible computing, in which virtually no dissipation scenario can be achieved.

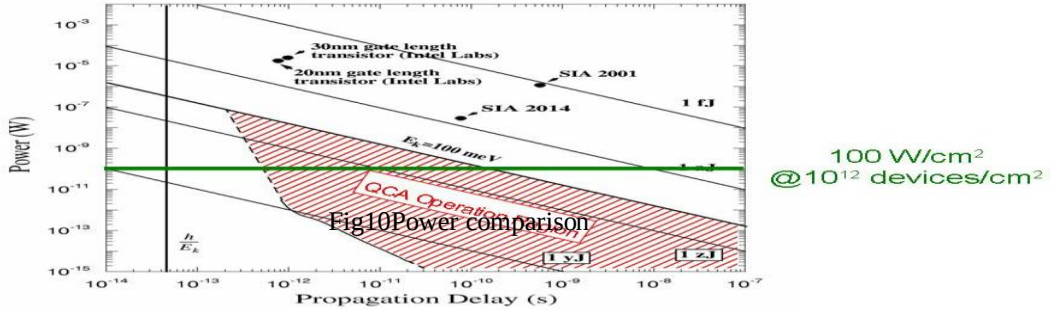

Fig10Power comparison

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4.3 density comparisons

Table 1

Technology	Length	Width	Area	Density Gain
CMOS (0.07 μ)	29.8 μm	45.5 μm	1356.1 μm^2	N/A
CMOS (0.05 μ)	32.5 μm	21.3 μm	692.3 μm^2	N/A
QCA ("conventional")	28.1 μm	2.7 μm	75.9 μm^2	17.8 (0.07 μ) / 9.1 (0.05 μ)
QCA ("molecular")	2.81 μm	0.27 μm	7.6 μm^2	1787 (0.07 μ) / 912 (0.05 μ)

4.4 limitations

According to the Technology Roadmap for Nanoelectronics , there are two main problems that must be overcome to successfully implement a QCA circuit. They are the need for individual adjustment of each cell and the limits of operating temperature. Individual adjustment of each cell is currently required because of fabrication tolerances, the presence of stray charges, and need for 4N + 2 excess electrons in each cell (limits performance degradation). To make cell adjustment possible, leads are required to load onto the quantum dots the exact and required number of excess electrons. By attaching leads to cells, straightforward lateral branching from a chain of cells (a basic feature needed to create logic gates) is prevented .Operating temperature limitations are more fundamental in nature . Operating temperature limits stem from the weakness of the dipole interactions between cells which much be significant larger than kT. The current state of the art in QCA devices is the majority gate. This gate was constructed based on metal-insulator tunnel junctions which operate at only a few millikelvin. Structures at the molecular level will be needed to approach room temperature operation.

Table 2 Projections for QCA in various benchmarks

Benchmark	2006	2012
Feature size	2 nm	10 nm
No. of devices	4	10^6
Circuit speed	10 kHz	100 GHz
Events / chip / s	4 10^4	10^{14}
Power supply, V_{dd}	0.1 mV	0.1 mV
Power dissipation	1 pW (excluding cooling)	n/A
Temperature	4 K	4 K

V. Introduction to VLSI

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistor-based circuits into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into the hundreds of millions of transistors.

5.Introduction about verilog

In the semiconductor and electronic design industry, Verilog is a hardware description language (HDL) used to model electronic systems. Verilog HDL, not to be confused with VHDL (a competing language), is most commonly used in the design, verification, and implementation of digital logic chips at the register-transfer level of abstraction. It is also used in the verification of analog and mixed-signal circuits.

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VI. spartan3efpgakit

6. Introduction

The Basys2 board is a circuit design and implementation platform that anyone can use to gain experience building real digital circuits. Built around a Xilinx Spartan-3E Field Programmable Gate Array and a Atmel AT90USB2 USB controller, the Basys2 board provides complete, ready-to-use hardware suitable for hosting circuits ranging from basic logic devices to complex controllers. A large collection of on-board I/O devices and all required FPGA support circuits are included, so countless designs can be created without the need for any other components

Four standard expansion connector allow designs to grow beyond the Basys2 board using breadboards, user-designed circuit boards, or Pmods (Pmods are inexpensive analog and digital I/O modules that offer A/D & D/A conversion, motor drivers, sensor inputs, and many other features). Signals on the 6-pin connectors are protected against ESD damage and short-circuits, ensuring a long operating life in any environment. The Basys2 board works seamlessly with all versions of the Xilinx ISE tools, including the free WebPack. It ships with a USB cable that provides power and a programming interface, so no other power supplies or programming cables are required.

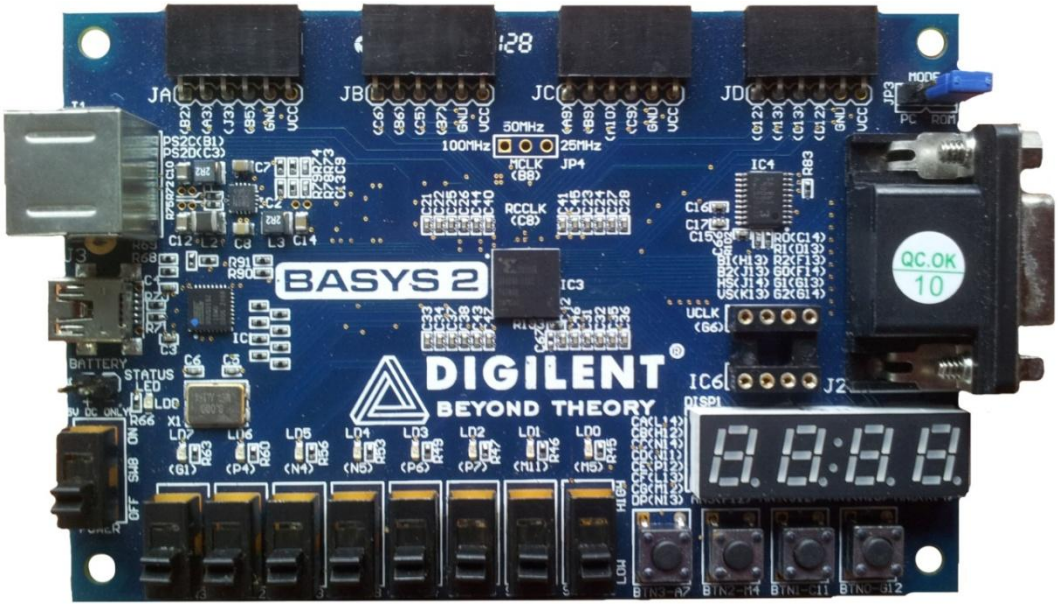

Fig 11 Basys2 FPGA BOARD

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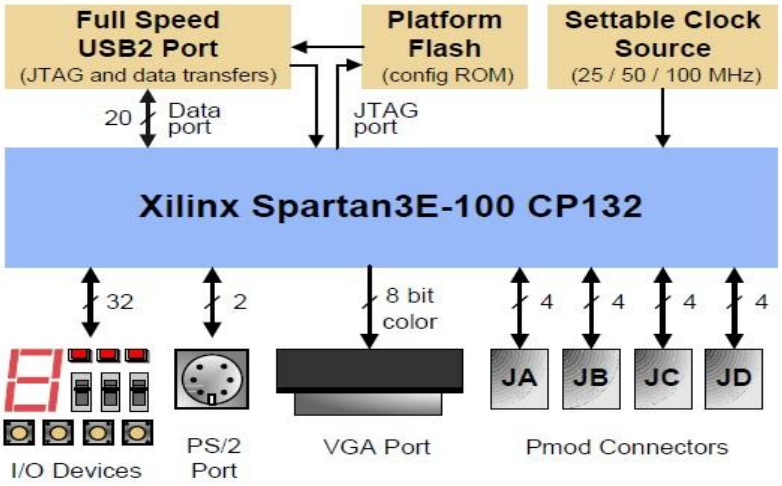

Fig 12 Basys2 board block diagram and features

VII. Result And Analysis

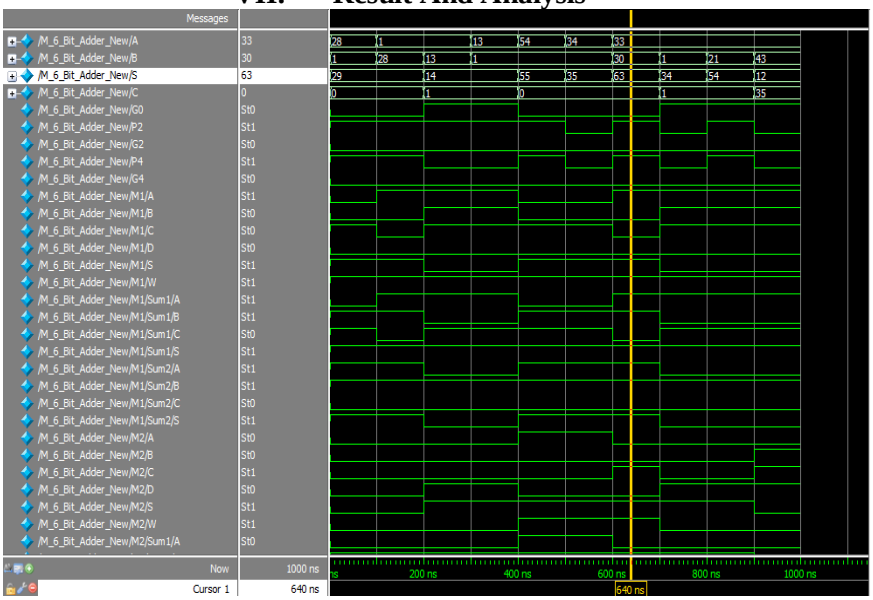

Fig 13 1 6 bit Adder Output

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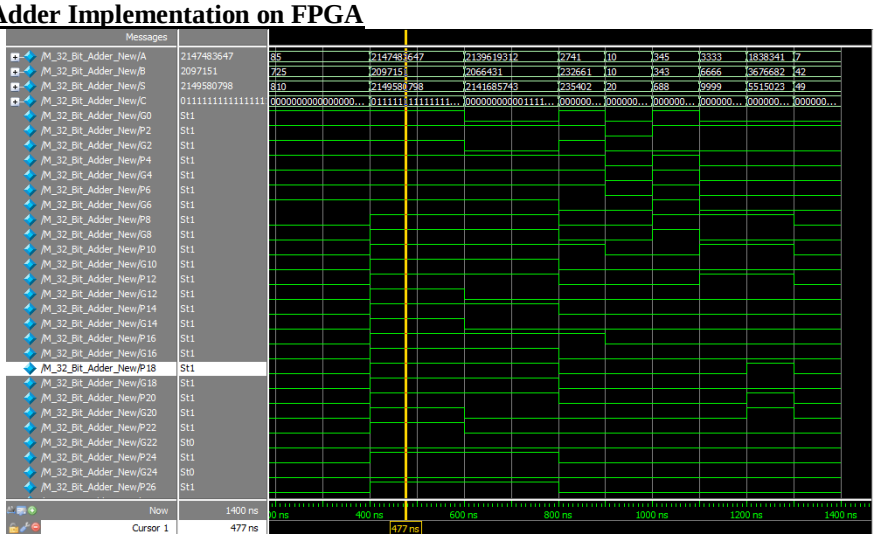

Fig 14 32 bit Adder Output

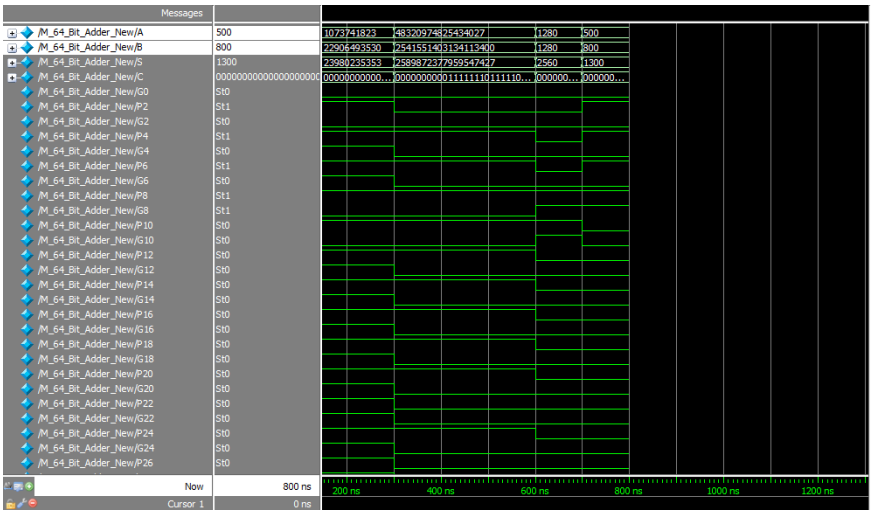

Fig 15 64 bit Adder Output

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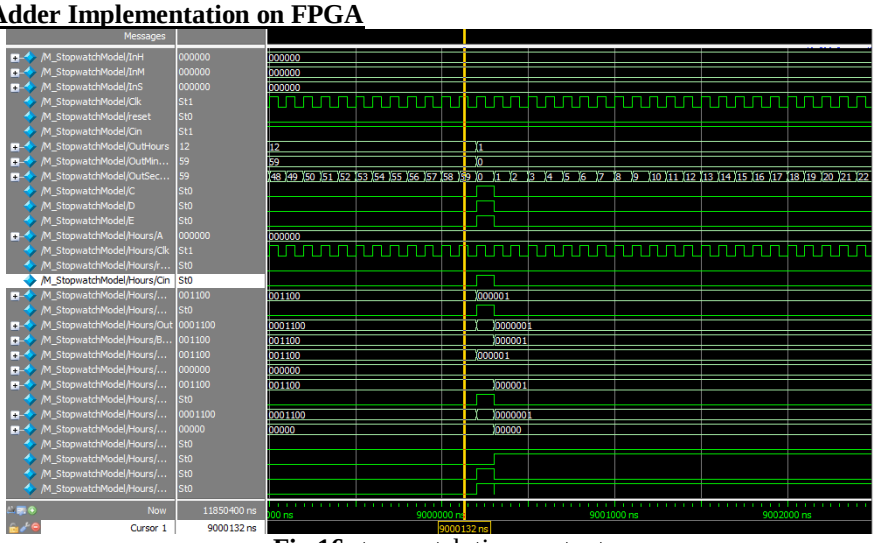

Fig 16 stop-watch timer output

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of 4 input LUTs	30	7,168	1%	
Logic Distribution				
Number of occupied Slices	21	3,584	1%	
Number of Slices containing only related logic	21	21	100%	
Number of Slices containing unrelated logic	0	21	0%	
Total Number of 4 input LUTs	30	7,168	1%	
Number of bonded IOBs	48	141	34%	
Total equivalent gate count for design	183			
Additional JTAG gate count for IOBs	2,304			

Fig 17device utilization summary

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Author Profile

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